REMARKS

Claims 1, 3–6, 8–11, 13–14 and 16–19 are pending in the present application.

Claims 4 and 14 were amended solely to correct typographical and grammatical errors within those claims.

The specification has been amended to correct errors therein. No new matter has been added to the specification.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 6 and 9 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

Claims 6 and 9 have been amended to correct the errors identified in the Office Action.

Therefore, the rejection of claims 6 and 9 under 35 U.S.C. § 112, second paragraph has been overcome.

AMENDMENTS WITH MARKING TO SHOW CHANGES MADE

The paragraph labeled "CROSS REFERENCE TO RELATED APPLCIATIONS" inserted on page 1 and line 1 of the specification by amendment mailed October 12, 2001 was amended herein as follows:

This application is a continuation application of prior application Ser. No. 09/127,050 filed July 31, 1998, now abandoned.

The clauses on page 5 at lines 10–12 of the specification was amended herein as follows:

FIGURE 3A is a more detailed diagram and top view of the conductor set forth in FIGURE [3]2;

FIGURE 3B is a cross-sectional view along line [A-A]3B–3B of FIGURE 3A;

The paragraph on page 7 at line 7 was amended herein as follows:

In general terms, a signal on one conductor increasing in voltage while a signal on another conductor decreases in voltage (resulting in an increase in the

voltage difference or "delta" votlage over time) generates the maximum capacitve efect, while two signals increasing (or decreasing) together generated the least capacitive effect. In other words, the capacitive effect is great between non-shielded conductor lines when both signals are active and opposite in direction. This effect remains substantial when one signal is active (increasing or decreasing) and the other signal is static (e.g., one signal is rising to a logic one and the other signal is held at a logic zero).

The paragraph on page 10 at lines 13–17 of the specification was amended herein as follows:

As shown in FIGURE 4C, the conductors 120b and 120c could also be utilized by other circuitry (connected as indicated in the figure by the label "TO OTHER CIRCUITRY") when the conductor 120a is not active, unused, or when a signal is transmitted whose speed or propagation delay is unimportant. This is accomplished using switches and/or tri-state devices with appropriate control lines, and can be implemented by those skilled in the art.

Claims 6 and 9 were amended herein as follows:

6. (amended) The apparatus in accordance with Claim 5 wherein [the first conductor and] the fourth conductor [are]is located substantially in a second plane.

9. (amended) The apparatus in accordance with Claim 1 wherein the electrical signal comprises a clock signal, and wherein the apparatus reduces the propagation delay of [a]the clock signal when transmitted on the first conductor.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 7-16-02

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